WHAT IS CLAIMED IS:

1. An integrator stage for use in a delta sigma modulator comprising:

an operational amplifier;

an integration capacitor coupling an output of the operational amplifier and a summing node at an input of the operational amplifier;

first and second feedback paths each including switching circuitry for selectively sampling a reference voltage onto a first plate of a corresponding capacitor during a sampling phase, a second plate of the capacitors of the feedback paths being coupled in common at a common plate node; and

a switch for selectively coupling the common plate node and the summing node during an integration phase.

2. The integrator stage of Claim 1 and further comprising:

a second integration capacitor coupling a second output of the operational amplifier with a second summing node at a second input of the operational amplifier;

third and fourth feedback paths each including switching circuitry for selectively sampling the reference voltage onto a first plate of a correponding capacitor during the sampling phase, a second plate of the capacitors of the third and fourth feedback paths coupled in common at a second common plate node, the third and fourth feedback paths sampling the reference voltage differentially with respects to the first and second feedback paths; and

a second switch for selectively coupling the second common plate node and the second summing node during the integration phase.

3. The integrator stage of Claim 1 wherein the switching circuitry comprises switches for selectively coupling and cross-coupling first and second reference voltage inputs of the corresponding feedback path in response to a control signal.

4. A delta sigma modulator comprising:

a loop filter comprising an integrator stage, the integrator stage comprising:

an operational amplifier;

an integration capacitor coupling an output of the operational amplifier and a summing node at an input of the operational amplifier; and

a mutiple-bit digital to analog converter comprising:

first and second capacitors having first plates coupled in common at a common node;

switching circuitry for selectively sampling a selected reference voltage onto a second plate of a corresponding one of the capacitors during a sampling phase; and

switching circuitry for selectively coupling the common node with the summing node during an integration phase.

5. The delta sigma modulator of Claim 4 further comprising:

a output summer coupled to outputs of the loop filter in a feedforward configuration; and

a feedforward path of a selected gain coupling a loop filter input and the output summer for canceling an input signal energy into the loop filter input.

6. The delta sigma modulator of Claim 5 further comprising a quantizer for feeding-back a control signal to the switching circuitry of the digital to analog converter, a gain of the feed-forward path inversely proportional to gains of the quantizer and the digital to analog converter.

5

7. A delta sigma modulator comprising:

a plurality of filter stages having outputs coupled to inputs of an output summer;

a feedback loop coupled to an output of the output summer and having a gain for feeding-back control signals to at least one of the filter stages; and

a feed-forward path coupling an input of the modulator and an input of the output summer and having a gain approximately inversely proportional to the gain of the feedback loop.

8. The delta –sigma modulator of Claim 7 wherein the feedback loop comprises a quantizer and a DAC and the gain of the feed-forward path is approximately:

1/quantizer gain * 1/ DAC gain.

9. The delta – sigma modulator of Claim 7 wherein a selected one of the filter stages comprises an integrator stage comprising:

an operational amplifier and an associated integration capacitor;

input signal switching circuitry for sampling an input signal charge onto an input sampling capacitor during a sampling phase and transferring the input signal charge to a common node during a first period of an integration phase;

reference voltage switching circuitry including switches controlled by a plurality of control signals generated by the feedback loop for sampling a reference charge onto a plurality of reference sampling capacitors during the sampling phase and transferring the reference charge to the common node during the first period of the integration phase; and

summing switches for transferring charge from the common node to the integration capacitor during a second period of the integration phase.

10. The delta-sigma modulator of Claim 9 wherein selected plates of selected ones of the plurality of reference sampling capacitors are coupled electrically in common.

11. The delta sigma modulator of Claim 8 further wherein the feedback loop further comprises dynamic element matching logic coupling the quantizer and the DAC.

12. The delta sigma modulator of Claim 9 wherein the switches of the reference voltage switching circuitry selectively couple the reference sampling capacitors to a selected one of first and second reference voltage rails.

13. The delta sigma modulator of Claim 9 wherein the input signal switching circuitry samples the input signal charge in rough and fine subphases of the sampling phase.

14. The delta sigma modulator of Claim 9 wherein the reference voltage switching circuitry samples the reference voltage in rough and fine subphases of the sampling phase.

15. The delta sigma modulator of Claim 9 wherein the control signals are generated during the integration phase of a first operational cycle to configure the switches of the reference switching circuitry prior to the sampling phase of a second following operational cycle.

16. A method of operating a switched capacitor integrator comprising the steps of:

during a sampling phase selectively sampling a reference voltage of a selected polarity onto an input plate of a reference capacitor in response to a control signal;

during the sampling phase selectively sampling an input signal voltage onto an input sampling capacitor;

during a first period of an integration phase, transferring the sampled voltages from the reference and input sampling capacitors to a common node; and

during a second period of the integration phase, transferring the sampled voltages from the common node to an integration capacitor.

17. The method of Claim 16 further comprising the step of generating the control signal during an integration phase preceding said step of sampling the reference voltage.

18. A method of operating a delta-sigma modulator including a loop filter having a plurality of outputs feeding-forward filter output signals into an output summer and a feedback loop for coupling a feedback signal from an output of the summer to an input of the loop filter comprising the step of:

feeding-forward an input signal through a feed-forward path from a modulator input to the output summer with a selected gain for canceling input signal energy into the modulator.

19. The method of Claim 18 wherein said step of feeding-forward comprises the substeps of:

disconnecting an input stage of the loop filter input from the modulator input; and

subsequently disconnecting the feed-forward path from the modulator input.

20. The method of Claim 19, wherein the feed-forward path is disconnected after the feedback path generates the feedback signal.

21. A method of interconnecting paths and an integration capacitor in a switched-capacitor integrator comprising the steps of:

coupling top plates of first and second reference capacitors of first and second reference paths of a selected polarity together at a common node; and

coupling a switch between the common node and the integration capacitor for selectively coupling the common node to the integration capacitor.

22. The method of interconnecting of Claim 21 and further comprising the step of providing switches for selectively coupling input plates of the reference capacitors to a reference voltage of a selected polarity.

23. The method of interconnecting of Claim 21 further comprising the step of coupling a top plate of an input signal sampling capacitor to the summing node.

24. A method of operating a delta sigma modulator comprising a loop filter including an integrator stage, a quantizer, first and second capacitors having common first plates, first switching circuitry for selectively sampling a selected reference voltage to a second plate of the each of the capacitors in response to a control signal generated by the quantizer, and second switching circuitry for transfering charge from the common first plates of the capacitors to the input of the integrator stage, comprising the steps of:

during a first sampling phase, sampling selected reference voltages to the second plates of the capacitors with the first switching circuitry in response to a first control signal generated by the quantizer during a prior integration phase;

during a first integration phase performing the substeps of:

selectively transfering charge from the common first plates of the first and second capacitors to the input of the integrator stage with the second switching circuitry; and

generating a second control signal with the quantizer; and

during a second sampling phase, sampling selected reference voltages to the second plates of the capacitors with the first switching circuitry in response to the second control signal generated by the quantizer.

25. The method of Claim 24 wherein said step of transferring charge from the first common plates of the capacitors to the input of the integrator stage comprises the step of transfering charge to a selected one of first and second differential inputs to the integrator stage.

26. The method of Claim 25 and further comprising the step of passing the first and second control signals generated by the quantizer through dynamic element matching logic prior to presentation to the first switching circuitry.

27. The method of Claim 25 wherein said integration phase further comprises the step of forcing charge from the second plates of the capacitors to the common first plates of the capacitors by reversing a voltage at the second plates of the capacitors prior to said step of selectively transferring charge from the common first plates to the input of the integrator.